Claims

1. A multiplierless IIR digital filter, comprising:

a memory having stored thereon power-of-two coefficients derived from a genetic algorithm;

a first shift register having an input to receive input samples;

a second shift register having an input to receive previous outputs;

a shifter stage in communication with the memory and the shift registers to receive the power-of-two coefficients, input samples, and previous outputs and perform a shift operation for corresponding power-of-two coefficients, input samples and previous outputs to thereby produce products; and

an adder stage, in communication with the shifter stage, to receive the products and provide a summation of the products.

2. The digital filter of claim 1, wherein the memory is a ROM.

3. The digital filter of claim 1, further comprising:

a first multiplexer in communication with the first shift register to receive the input samples; and

a second multiplexer in communication with the second shift register to receive the previous outputs.

4. The digital filter of claim 1, wherein the shifter stage includes barrel shifters with each barrel shifter performing a shift operation for a received power-of-two coefficient.

5. The digital filter of claim 4, wherein the shifter stage includes 32 barrel shifters.

6. The digital filter of claim 1, wherein the adder stage includes an adder tree having adder elements disposed in series.

7. The digital filter of claim 6, wherein each adder element includes an adder for receiving two values and providing a sum.

8. The digital filter of claim 6, wherein the adder stage includes two adder trees disposed parallel to one another to receive products from the shifter stage, each adder tree having adder elements disposed in series and each adder element having an adder for receiving two values and providing a sum.

9. The digital filter of claim 1, further comprising an accumulator in communication with the adder stage to receive values from the adder stage and provide a sum of the values.

10. The digital filter of claim 1, further comprising a controller in communication with the memory and the shift registers.

11. A method for filtering an input signal through multiplierless digital techniques, the method comprising:

generating power-of-two coefficients from a genetic algorithm;

storing the power-of-two coefficients in a memory;

receiving input samples representative of the input signal and previous outputs;

performing a shift operation to generate products by applying the power-of-two coefficients in accordance with a filter design to corresponding input samples and previous outputs; and

adding the products in parallel to provide sums of the products.

12. The method of claim 11, wherein receiving the input samples and previous outputs includes storing the input samples in a first register and storing the previous outputs in a second register.

13. The method of claim 12, wherein receiving the input samples and previous outputs further includes receiving the input samples in a first multiplexer and receiving the previous outputs in a second multiplexer.

14. The method of claim 11, wherein the memory is a ROM.

15. The method of claim 11, wherein performing a shift operation includes barrel shifters shifting the input samples and previous outputs based on corresponding power-of-two coefficients.

16. The method of claim 11 wherein adding the products in parallel includes disposing adder elements in series, each adder element having an adder for receiving two values and providing a sum.

17. The method of claim 11, further comprising accumulating the sums of the products to provide an output.

18. A multiplierless IIR digital filter, comprising:

a memory having stored thereon power-of-two coefficients derived from a genetic algorithm;

a first shift register to receive input samples;

a second shift register to receive previous outputs;

a shifter stage in communication with the memory and the first and second shift registers, and including barrel registers to each perform a shift operation for corresponding power-of-two coefficients, input samples, and previous outputs to thereby produce products;

an adder stage in communication with the shifter stage, and including adder trees, each adder tree having a series of adder elements to add the products in parallel and provide sums of the products; and

an accumulator in communication with the adder stage to add the sums of the products and produce an output.

19. The digital filter of claim 18, wherein the memory is a ROM.

20. The digital filter of claim 18, further comprising:

a first multiplexer in communication with the first shift register to receive the input samples; and

a second multiplexer in communication with the second shift register to receive the previous outputs.

21. The digital filter of claim 18, wherein the shifter stage includes 32 barrel shifters.

22. The digital filter of claim 18, wherein the adder stage includes an adder tree having adder elements disposed in series.

23. The digital filter of claim 18, further comprising a controller in communication with the memory and the first and second shift registers.

24. A multiplierless IIR digital filter, comprising:

memory means for storing thereon power-of-two coefficients derived from a genetic algorithm;

shift register means for receiving the input samples and previous outputs;

shifter means, in communication with the memory means and the shift register means, for performing a shift operation for corresponding power-of-two coefficients, input samples and previous outputs to thereby produce products; and

adder means, in communication with the shifter stage, for receiving the products and providing a summation of the products.

25. The digital filter of claim 24, wherein the memory means includes a ROM.

26. The digital filter of claim 24, wherein the shift register means includes a first shift register means for receiving the input samples and a second shift register means for receiving the previous outputs.

27. The digital filter of claim 26 further comprising:

a first multiplexer means in communication with the first shift register means to receive the input samples; and

a second multiplexer means in communication with the second shift register means to receive the previous outputs.

28. The digital filter of claim 24, wherein the shifter means includes barrel shifters with each barrel shifter performing a shift operation for a received power-of-two coefficient.

29. The digital filter of claim 24, wherein the adder means includes an adder tree having adder elements disposed in series.

30. The digital filter of claim 29, wherein each adder element includes an adder for receiving two values and providing a sum.

31. The digital filter of claim 29, wherein the adder means includes two adder trees disposed parallel to one another to receive products from the shifter means, each adder tree having adder elements disposed in series and each adder element having an adder for receiving two values and providing a sum.

32. The digital filter of claim 24, further comprising accumulator means, in communication with the adder means, to receive values from the adder means and provide a sum of the values.

33. The digital filter of claim 24 further comprising controller means in communication with the memory means and the shift register means.